

# **GATE STRUCTURES HAVING SIDEWALL SPACERS USING SELECTIVE DEPOSITION AND METHOD OF FORMING THE SAME**

## **ABSTRACT OF THE DISCLOSURE**

5           Gate stacks with sidewall spacers having improved profiles to suppress or eliminate  
void formation between the gate stacks during gap-filling is disclosed, along with a method  
of forming the gate structures over a semiconductor substrate. A gate dielectric layer is  
formed on a semiconductor substrate. Then, a gate stack 24 having a sidewall is formed  
over the gate dielectric layer. The gate stack 24 comprises a conductive layer 28 and a hard  
10 mask 30 overlying the conductive layer 28. A liner 32 is selectively deposited over the gate  
stack 24 such that the liner 32 is deposited on the hard mask 30 at a rate lower than the rate  
of deposition on the conductive layer 28. Thus, the liner 32 is substantially thinner on the  
hard mask 30 than on the conductive layer 28. A nitride spacer is formed over 34 the liner  
32. A PMD layer is formed over the resultant structure, filling the gaps between adjacent  
15 gate stacks and substantially free of voids.